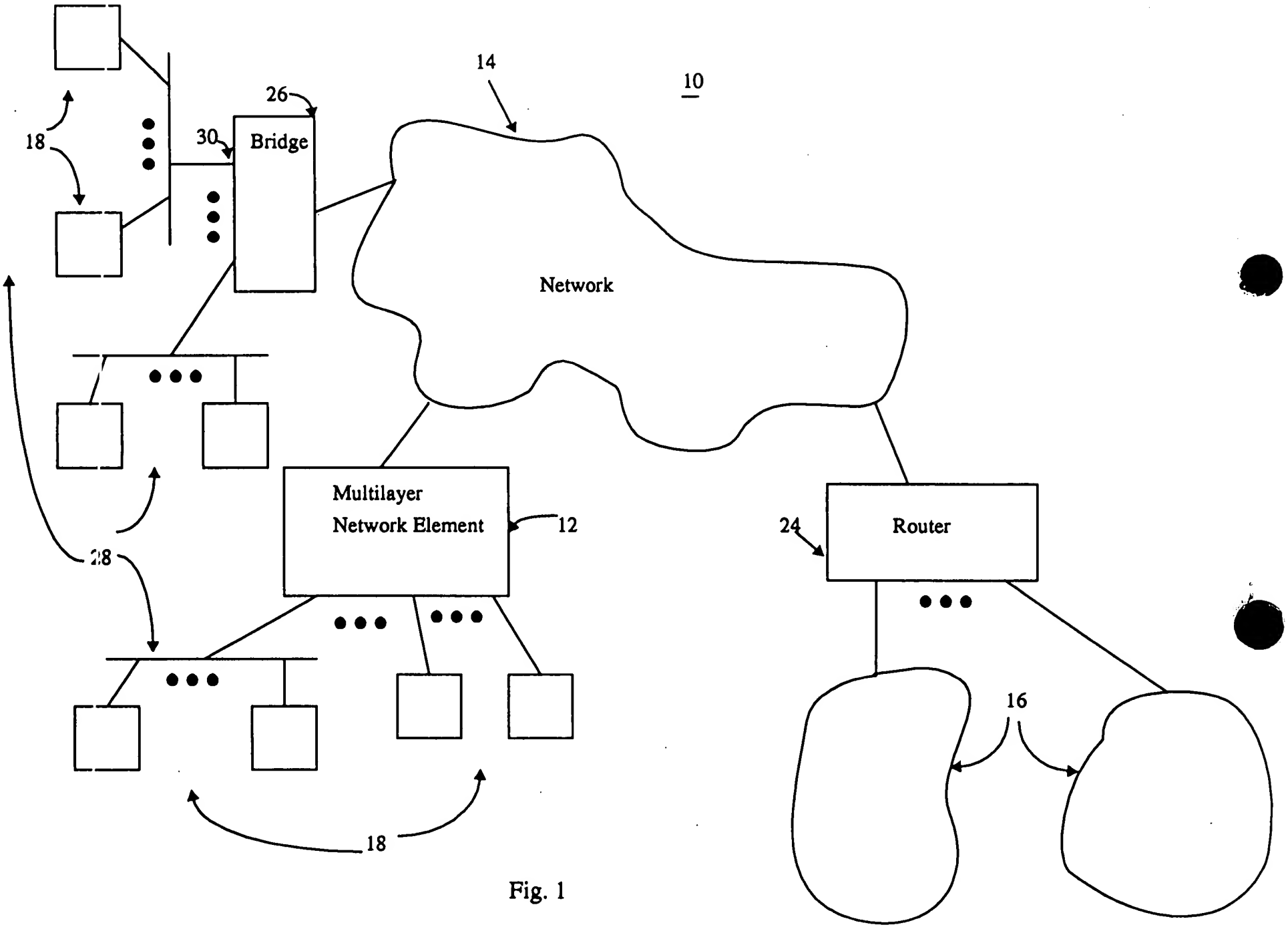
14
10
26
18
30
Bridge
Network
Multilayer
Network Element
12
24
Router
28
16
18

Fig. 1

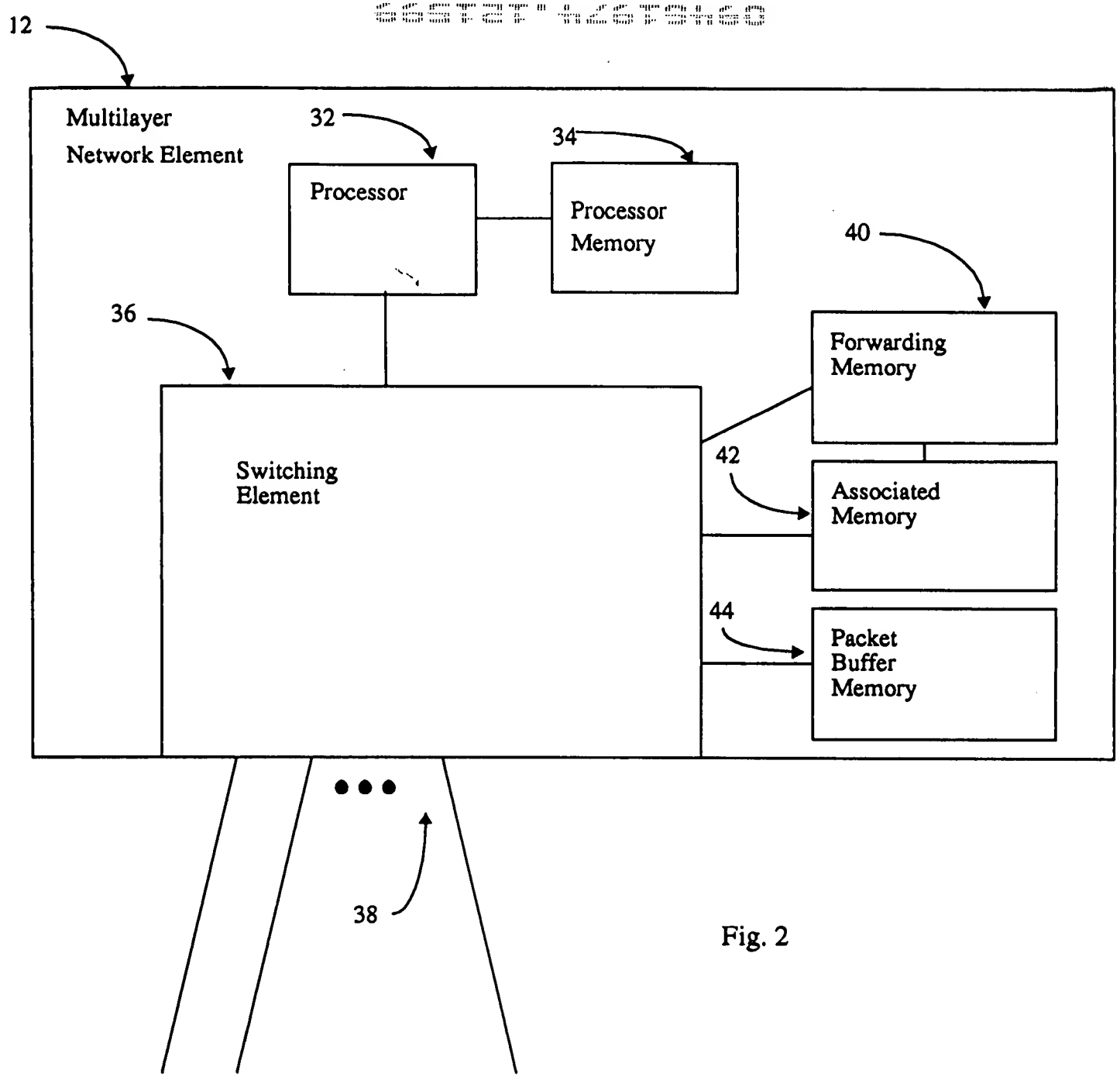
12
Multilayer
Network Element
32
Processor
34
Processor
Memory
40
Forwarding
Memory
36
Switching
Element
42
Associated
Memory
44
Packet
Buffer
Memory
38

Fig. 2

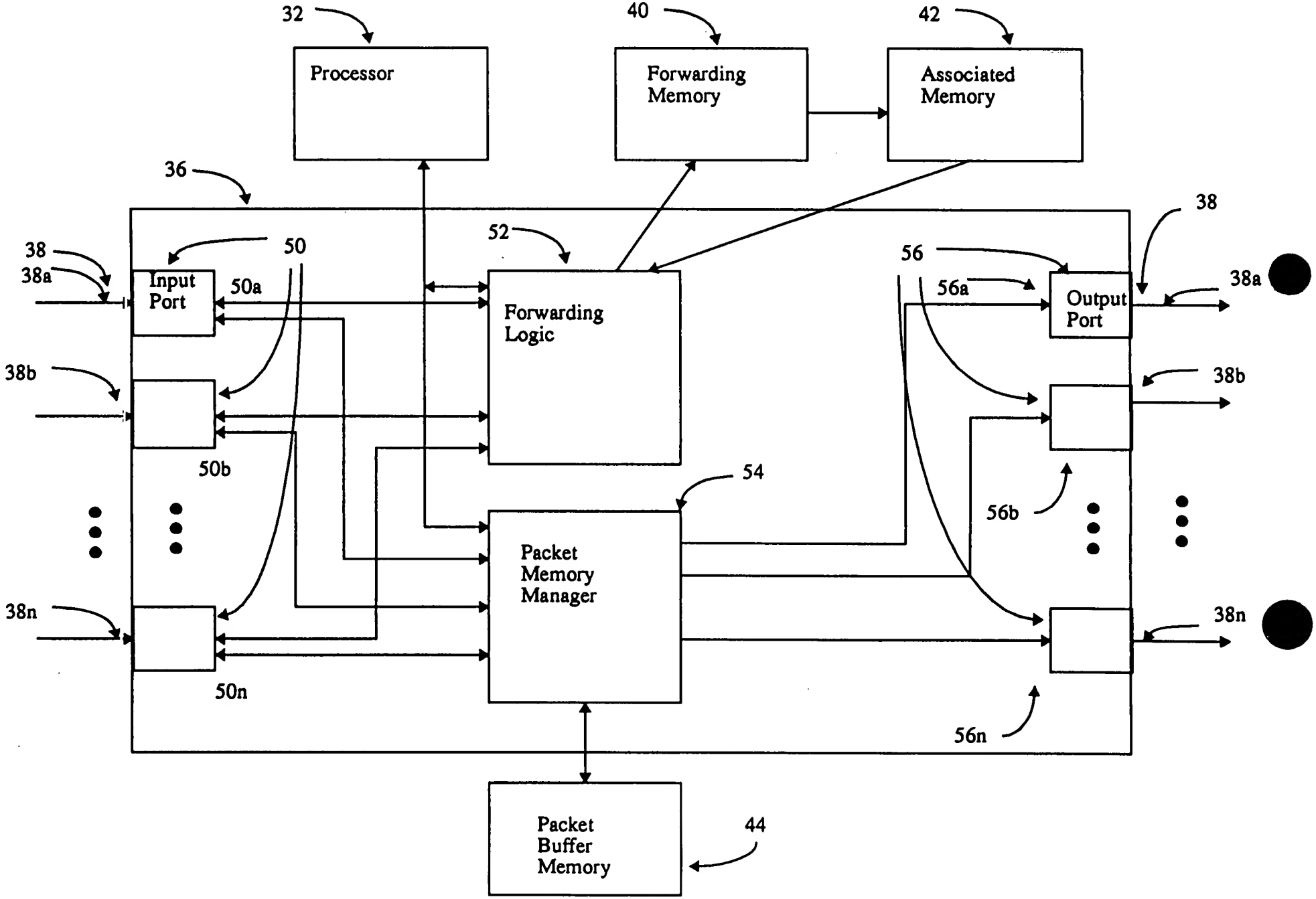
32
Processor
40
Forwarding Memory
42
Associated Memory
36
38
38a
50
Input Port
50a
52
Forwarding Logic
56
56a
Output Port
38a
38b
50b
38b
54
Packet Memory Manager
56b
38n
50n
38n
56n
Packet Buffer Memory
44

Fig. 3

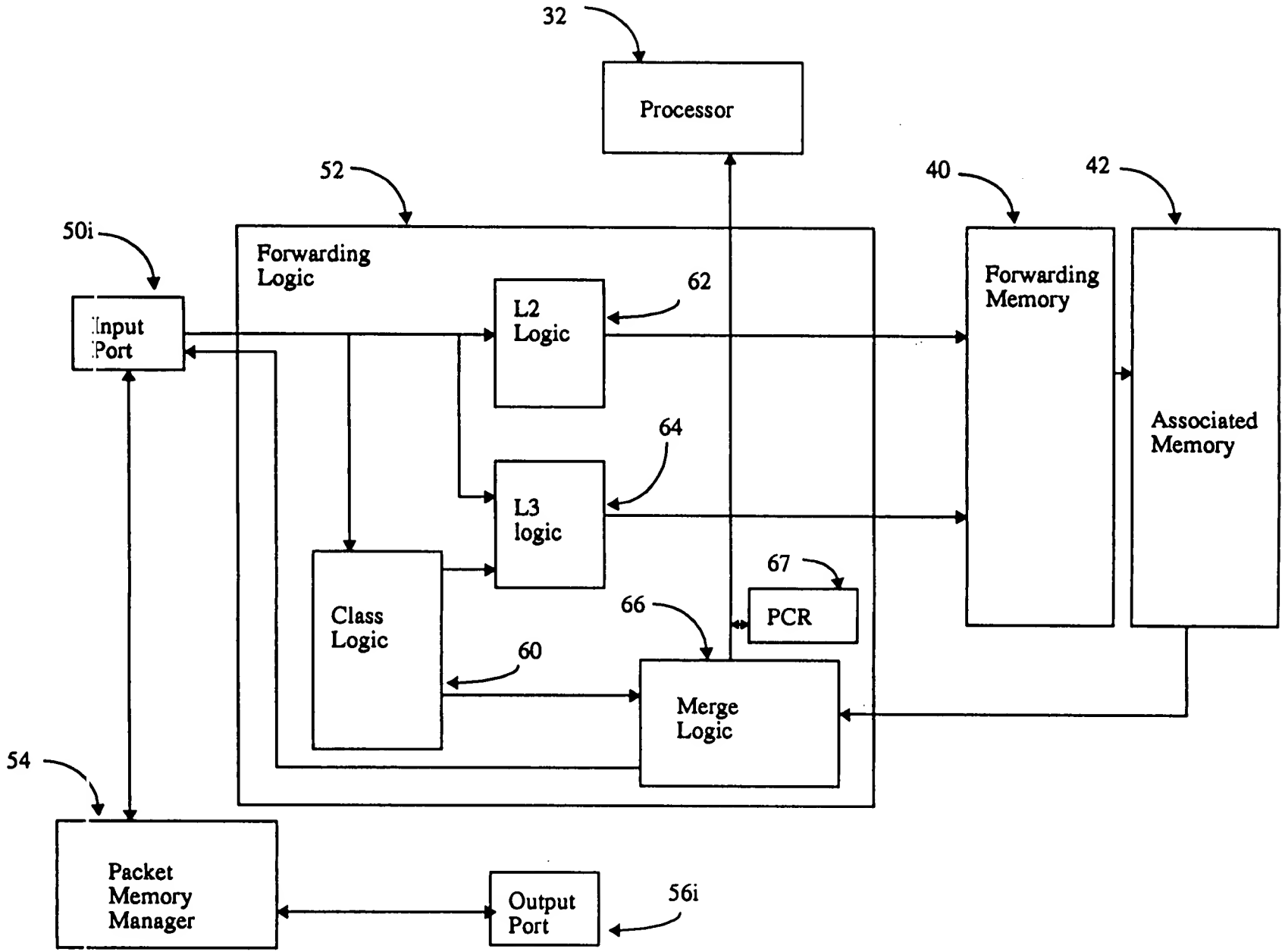
32
Processor
52
40
42
50i
Forwarding Logic
62
L2 Logic
Forwarding Memory
Input Port
Associated Memory
64
L3 logic
67
PCR
66
Class Logic
60
Merge Logic
54
Packet Memory Manager
Output Port
56i

Fig. 4

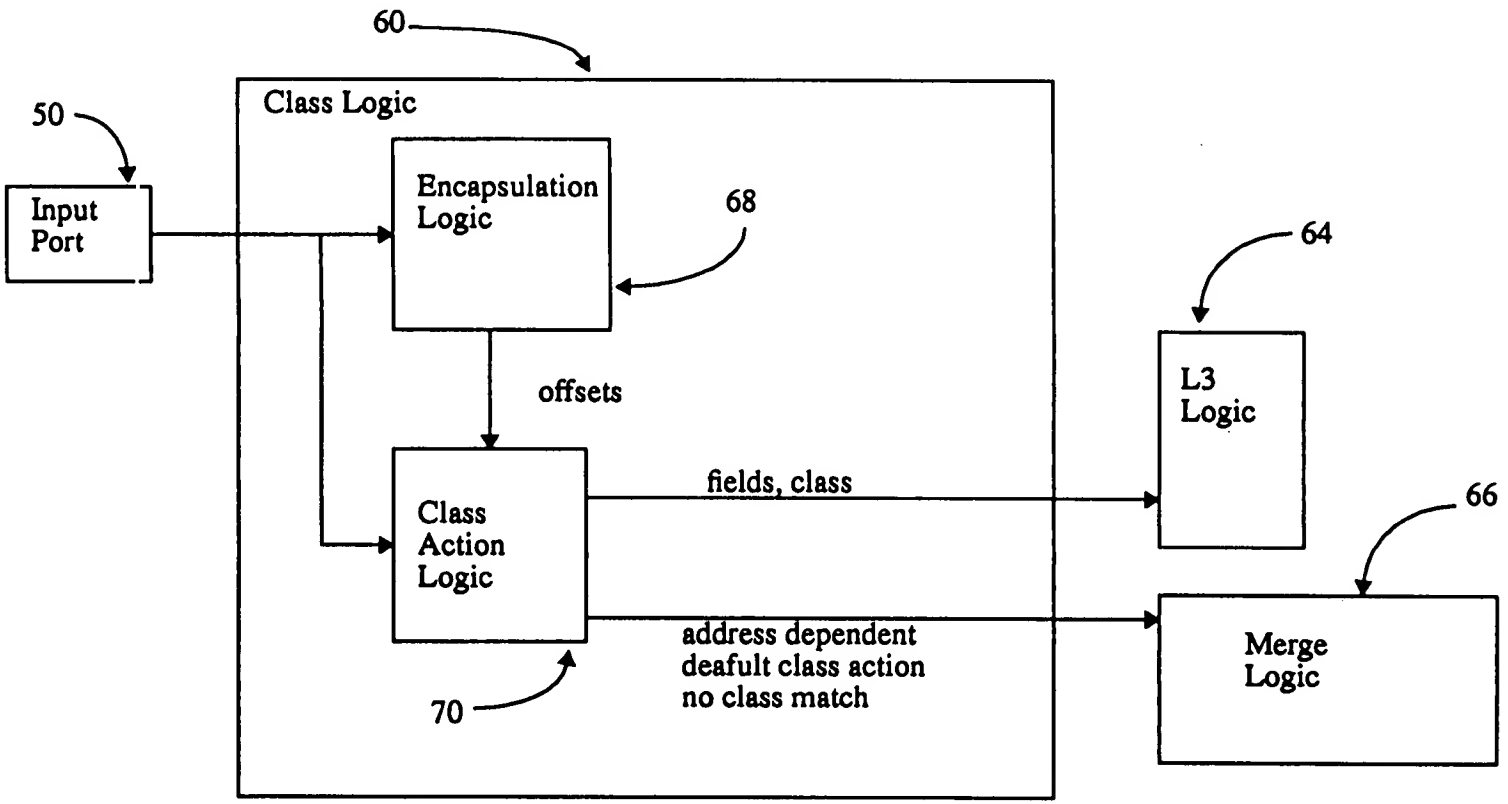
60
Class Logic
50
Input Port
Encapsulation Logic
68
64
L3 Logic
offsets
Class Action Logic
fields, class
66
Merge Logic
address dependent
deafult class action
no class match
70

Fig. 5

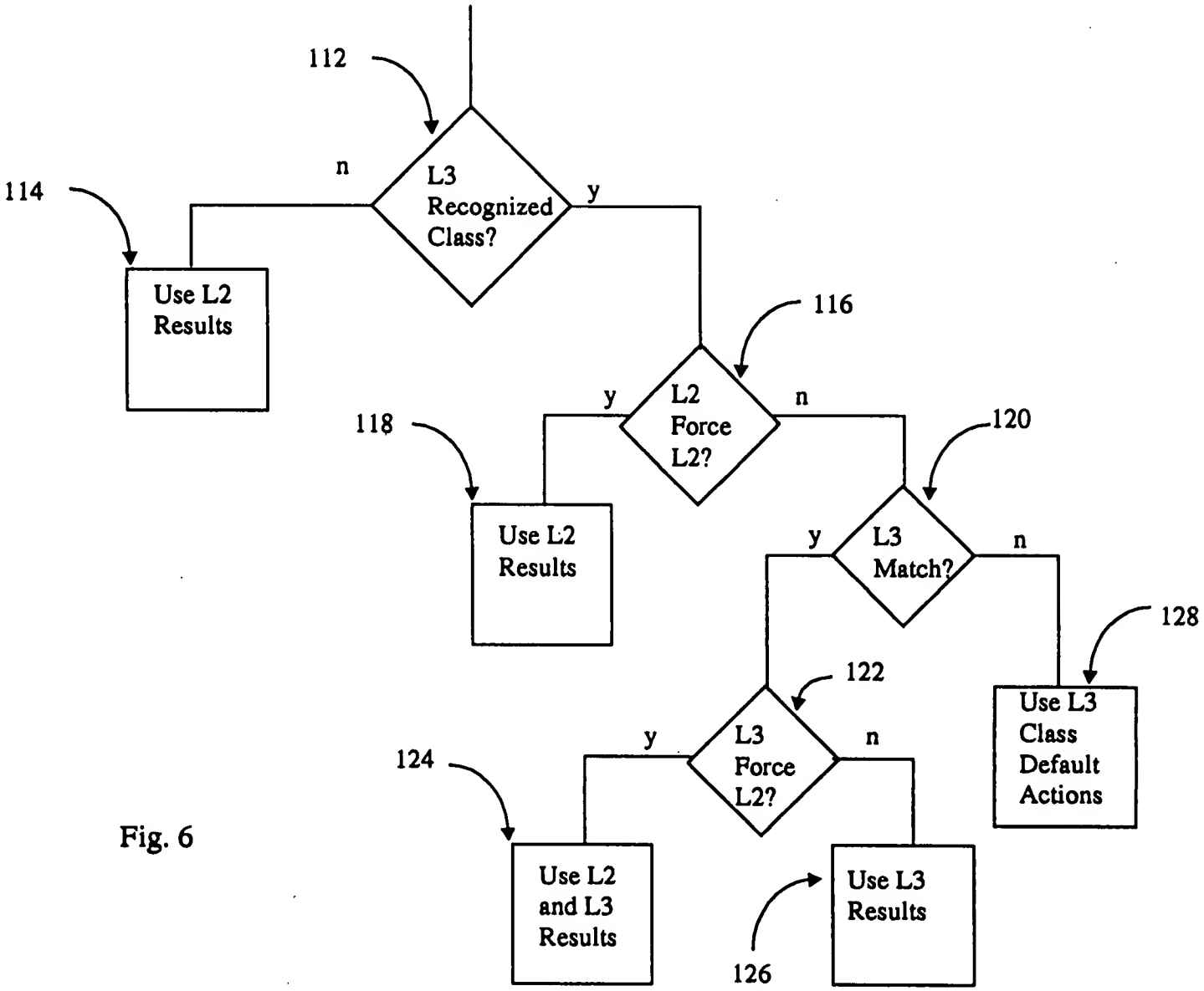
112
L3 Recognized Class?
n
y
114
Use L2 Results
116
L2 Force L2?
y
n
118
Use L2 Results
120
L3 Match?
y
n
128
Use L3 Class Default Actions
122
L3 Force L2?
y
n
124
Use L2 and L3 Results
126
Use L3 Results

Fig. 6

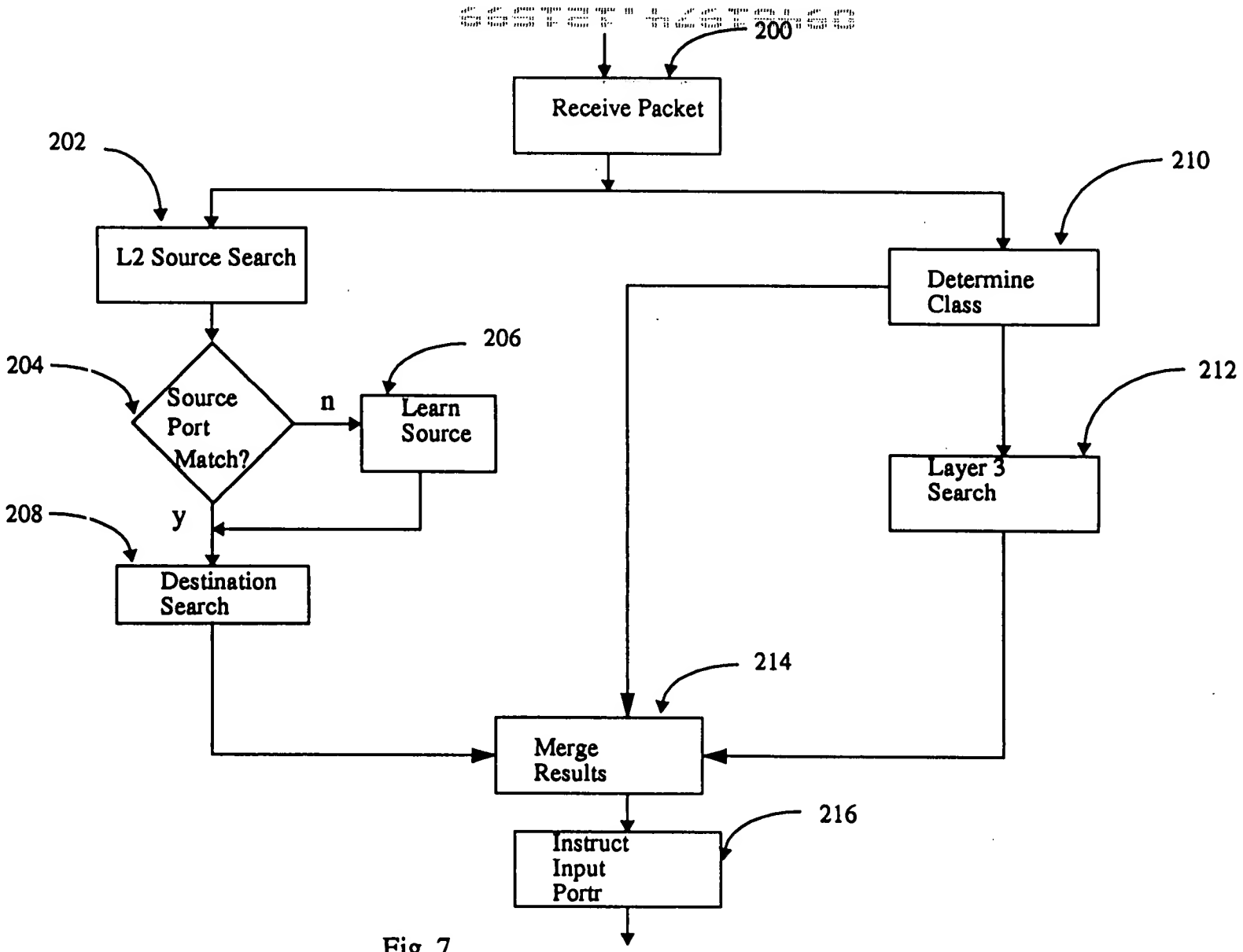
200
Receive Packet
202
L2 Source Search
210
Determine Class
204
Source Port Match?
n
206
Learn Source
212
Layer 3 Search
y
208
Destination Search
214
Merge Results
216
Instruct Input Portr

Fig. 7

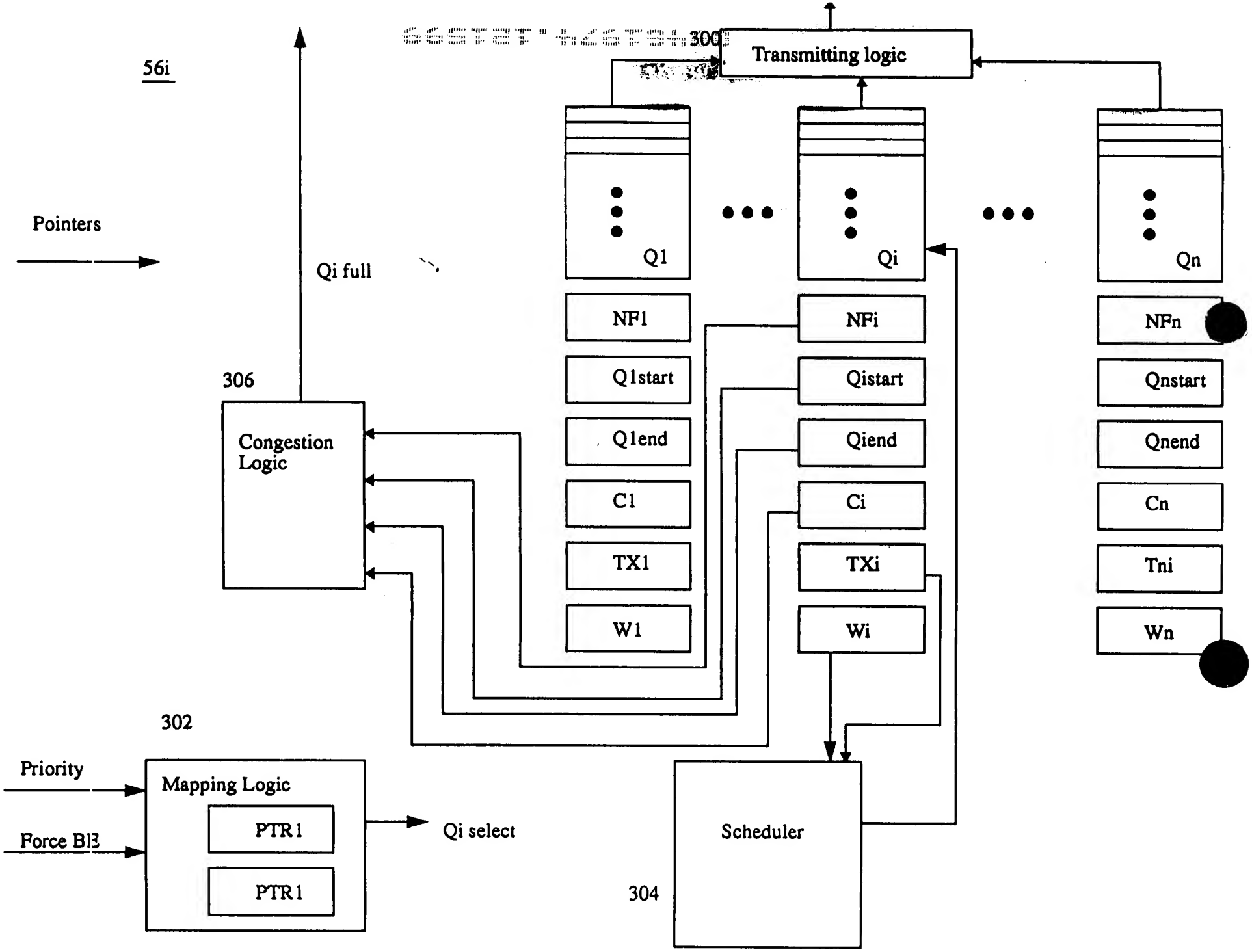
56i
Pointers
Qi full
300
Transmitting logic
Q1
Qi
Qn
NF1
NFi
NFn
Q1start
Qistart
Qnstart
Q1end
Qiend
Qnend
C1
Ci
Cn
TX1
TXi
Tni
W1
Wi
Wn
306
Congestion Logic
302
Priority
Force Bl3
Mapping Logic
PTR1
PTR1
Qi select
Scheduler
304

Fig. 8